Amendments to the Specification

Please replace paragraph **[0006]** of the specification with the following paragraph:

Additionally, it is equally important that non-overlapping clock edges be evenly distributed to all ~~corners~~ corners of a chip regardless of the distance which those signals must travel. As chip size increases, clock signals $\varphi 1$ and $\varphi 2$ have to travel greater distances throughout the chip. This causes clock signals $\varphi 1$ and $\varphi 2$ to become degraded. As distances increase, rising edges 202, 206 and failing edges 204, 208 may become obscured (experience phase shifts and increases in transition times) and can overlap. This phenomenon, sometimes referred to as clock skew, is caused by a number of factors, including: loading, unwanted noise, coupling, capacitance, resistance, inductance and other debilitating effects.

Please replace paragraph **[0007]** of the specification with the following paragraph:

To account for these factors, designers must separate the rising and falling edges 202, 204, 206, 208 of different clock signals (i.e., $\varphi 1$ and $\varphi 2$) with a large enough margin of time to allow for clock skew. For instance, failing edge 204 and rising edge 206 must be separated by a minimum temporal distance or amount of time ([[7]] T) to avoid overlapping states; especially for level-triggering operations in metal-oxide-silicon (MOS) technology. The larger T is, the less likely the chip will fail due to overlapping signals caused by skewing. The wide range of operating environments to which the chip(s) may be subject must be considered in selecting T. Therefore, to provide an adequate margin, manufacturers are forced to select T large enough to provide functionality in a worst-case environment. However, a large T is a significant cycle time constraint. Therefore chip design is not optimized for each environment.

Please replace paragraph **[0012]** of the specification with the following paragraph:

The programmable on-chip clock generator provides two phases of a system clock with non-overlapping edges. The ~~programmability~~ programmability of the clock generator provides flexibility during chip fabrication, and when a chip is functioning in a operational environment.

Please replace paragraph **[0018]** of the specification with the following paragraph:

FIG. 2A illustrates two clock signals identified by [[0]] φ1 and [[0]] φ2 with nonoverlapping edges.

Please replace paragraph **[0019]** of the specification with the following paragraph:

FIG. 2B illustrates three possible states for clock signals [[0]] φ1 and [[0]] φ2.

Please replace paragraph **[0033]** of the specification with the following paragraph:

Chip 304 also has an internal clock generator 308, which provides multiple clock signals to elements 310. In a preferred embodiment clock generator 308 provides two clock signals, φ1 and φ2; similar to FIG. 2A. To ensure ~~4hat~~ that active portions of clock signals φ1 and φ2 are non-overlapping, clock generator 308 is programmed to achieve optimal non-overlapping clock generation. Accordingly, clock generator 308 provides a plurality of programmable non-overlapping times between clock signals φ1 and φ2. In the preferred embodiment, clock generator 308 provides the option of selecting between 0.5ns, 2.5ns and 4.5ns of non-overlapping time between clock signals φ1 and φ2 shown as T in FIG. 2A. In alternative embodiments, T must be less than the period of CLKIN 401. Furthermore, for a 50 % duty cycle T should be less than the period of CLKIN/2. If this condition is not met, the circuit may chop out clocks.

Please replace paragraph **[0038]** of the specification with the following paragraph:

Referring now to FIGS. 4 and 5, in a step 502, clock generator 308 receives an external clock signal 401 from external clock 302 shown as "CLKIN" 401 (as shown in FIG.4). In a step 504, input waveform[[.]] stabilizer 02 stabilizes CLKIN 401. Waveform stabilizer 402 reshapes CLKIN 401 into a square wave (CLK 405) because CLKIN 401 tends to be distorted due to input jitter, noise from ground bounce and coupling. In the preferred embodiment, waveform stabilizer 402 is a Schmitt trigger. The structure and operation of a Schmitt trigger are well known to those skilled in the art.

Please replace paragraph **[0045]** of the specification with the following paragraph:

Referring to FIG. 6B, time adjuster 406 operates as follows. An input clock signal (CLK) 405 passes through inverter 609 to form inverted clock signal 601 (NOTCLK 601). CLK 405 and NOTCLK 601 are used to form two new clock signals φ1 and φ2. CLK 405 is an input signal to NOR gate 602 along with a delayed signal φ2. NOTCLK 601 is an input signal to NOR gate 603 along with delayed [[0]] φ1 signal.

Please replace paragraph **[0048]** of the specification with the following paragraph:

As a result of delay τl, the rising transition of φ2 lags behind the falling transition of 451 by the amount of τl plus any gate delay times t. The amount of time separating the falling transitions of φ1 from the rising transitions of φ2 is controlled by adjusting τl. If the circuit designer wishes to increase the clock frequency, [[7-1]] $\underline{\tau l}$ is programmed to a lesser amount. On the other hand, if the circuit operation is hampered by overlapping falling and rising transitions of φ1 and φ2, respectively, τl is increased until this problem is rectified. In this manner, the circuit is optimized by increasing the clock frequency to the maximum permissible level without the transitions overlapping.